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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/24/2003

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EXAMINER

PAREKH, NITIN

ART UNIT

PAPER NUMBER

2811

DATE MAILED: 10/24/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/964,586

Applicant(s)

FRUTSCHY ET AL.

Examiner

Nitin Parekh

Art Unit

2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 05 September 2003.
- 2a) ☒ This action is FINAL. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-9 and 11-19 is/are pending in the application.
- 4a) Of the above claim(s) 11-19 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-9 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 28 September 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ 6) ☐ Other: _____

DETAILED ACTION

1. Newly amended claims 11-19 directed to an invention that is independent or distinct from the invention originally claimed for the following reasons:

Claims 11-19 including the limitations of the arrangement of the capacitor stiffener (see Fig. 9) are directed to the specie C of the Embodiment III (see Restriction Requirement- paper #3).

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 11-19 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Claim Objections

2. Claim 3 is objected to because of the following informalities:

Claim limitation "remote" as recited in claim 3, line 5, should read "remove".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claim 2 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The limitations as recited in claim 2, line 4 include: "plastic couplers arranged to mechanically secure, while electrically isolating...".

However, the description in the specification (see page 20, line 20 and page 14, line 9) and Figures 7 and 12 disclose the insulating couplers (730 and 730' respectively) being used to separate the power and ground portions.

Claim Rejections - 35 USC § 103

5. Claims 1, 4-7 and 9 insofar as being in compliance 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Dibene, II et al. (US Pat. 6452113) in view of Dibene, II et al. (US Pat. 6452804).

Regarding claim 1, Dibene, II et al. ('113 patent) disclose a microprocessor package having integrated circuits (IC)/an IC package comprising:

- a substrate (702 of an assembly 700 in Fig. 9 and 7) supporting the microprocessor/IC die (310 in Fig. 7; Col. 8, line 66), and
- a packaged circuit board (PCB)/package frame (602 in Fig. 6A/6B and 9) mounted/attached at a perimeter of the substrate (see Fig. 9 and Fig. 7) and arranged apart from the IC die on the substrate to deliver an electrical connection providing a low inductance power/current path to the die through the substrate (Col. 4, lines 25-28; Col. 8, lines 60-68; Col. 9, line 25)

(Fig. 6A-12; Col. 7, line 50- Col 10, line 25).

Dibene, II et al. ('113 patent) further teach the electrical connections/structure providing dual functions including a mechanical and electrical functions where the mechanical function includes the conductive interconnects providing a coupling/rigidity/support for the substrate (Col. 8, lines 50-60) and mechanical fasteners (802 in Fig. 9) proving the predetermined level of mechanical fastening/stiffening (Col. 9, lines 32-37).

Dibene II, et al. ('113 patent) fail to teach the PCB/package frame being a package stiffener concurrently providing a stiffening support.

Dibene, II et al. ('113 patent) further teach in another embodiment of Fig. 26, the PCB/package frame serving as a stiffener board for the assembly (Col. 15, lines 23-30).

Dibene, II et al. ('804 patent) teach an integrated circuit (IC) package having an interposer substrate (104 in Fig. 1) supporting the microprocessor/IC die (101 in Fig. 1) where a power regulator board/frame assembly (102/103 in Fig. 1) is mounted at a peripheral portion of the interposer substrate. Dibene, II et al. ('804 patent) further teach the assembly delivering a low inductance current, providing mechanical/fastening support to the interposer substrate (Col. 5, line 25; Col. 5, line 55) and also being functional as a stiffener board (Col. 6, lines 28-33) and electrically conductive frame assembly to provide a three dimensional Integrated architecture/configuration (Col. 5, line 53- Col. 7, line 25).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the PCB/package frame being the package stiffener concurrently providing a stiffening support as taught by the embodiment of Fig. 26 in Dibene, II et al. ('113 patent) and Dibene, II et al. ('804 patent) so that the mechanical coupling and the component support can be improved in Dibene, II et al's ('113 patent) package.

Regarding claims 4-6, Dibene II, et al. ('113 and '804 patents) teach substantially the entire structure as applied to claim 1 above, wherein Dibene II et al. ('113 patent) teach the substrate being a core substrate having a multiple internal layers in the IC- printed circuit board (IC-PCB) carrier package, the package having a variety of configurations including the flip chip ball grid/array device, built-up multilayer (BML), pinned grid array- PGA and ceramic land grid array (CLGA), etc. (Col. 9, lines 10-30; Col. 7, lines 25- 43).

Regarding claim 7, Dibene II, et al. ('113 and '804 patents) teach substantially the entire claimed structure as applied to the claim 1 above, wherein Dibene II et al. ('113 patent) further teach the PCB/package frame being made of an electrically conductive surfaces/sections using conventional circuit board fabrication processing including etching and metallization (Col. 8, lines 24-37) to withstand conditions/temperature of normal IC operation (Col. 3, 4 and 7-16), but Dibene II et al. ('113 and 804 patents) fail to teach using the frame being made of one of a stamped, etched, extruded and deposited frame.

Making or depositing the frame do not distinguish over Dibene II et al. regardless of the process for forming the frame, because only the final product is relevant, not the process of making such as "molding/stamping/etching, etc. or laminating ". Note that a

"product by process" claim is directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also *In re Brown*, 173 USPQ 685; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wertheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and *In re Marrosi et al.*, 218 USPQ 289, all of which make it clear that it is the patentability and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above case law makes clear. See also MPEP 706.03(e).

Regarding claim 9, *Dibene II, et al.* ('113 and '804 patents) teach substantially the entire claimed structure as applied to the claim 1 above, wherein *Dibene II et al.* ('113 patent) further teach a heat sink/heat spreader plate assembly (1006/1010/1004 in Fig. 10-11B) being bonded to/supported on the PCB/package frame (Col. 9, line 40-67).

6. Claims 2 and 3 insofar as being in compliance 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over *Dibene, II et al.* ('113 and '804 patents) as applied to claim 1 above, and further in view of *Dehaine et al.* (US Pat. 5925925).

Regarding claim 2, Dibene, II et al. ('113 and '804 patents) teach substantially the entire claimed structure as applied to claim 1 above, except the stiffener including a copper (Cu) ring split into power and ground portions having an insulating couplers arranged to mechanically secure, while electrically isolating the power and ground portions of the Cu ring.

Dibene, II et al. ('113 patent) further teach the PCB/package frame comprising:

- plated through-holes and electrically conductive surfaces/pads (610, 616A/B respectively in Fig. 6A/B; Col. 8, lines 25-50) being electrically connected to a conductive interconnect spacer having electrically conductive portions (612A/612B in Fig. 6A), the conductive layer/plating being copper (Cu)
- the conductive interconnect spacer providing dual functions including a mechanical support/coupling with the substrate and two separate conductive paths 616A and 616B in Fig. 6A/6B) including a first power path and a second ground path respectively in a coaxial arrangement (Col. 8, lines 50-68), and
- the electrically conductive portions of the conductive interconnect spacer being separated by an insulating dielectric portion/section (612 C in Fig. 6A; Col. 8, lines 37-47).

Dibene, II et al. ('113 patent) further teach in another embodiments of Fig. 13 and 14, a configuration of the power and ground conductive paths being provided in two concentric metal rings electrically isolated from each other (see 1306/1304 and

1404/1402 respectively in Fig. 13 and 14; Col. 10, lines 35- Col. 11, line 15) or using a plurality of two piece coaxial conductive interconnects at the corners of the IC die (Col. 9, lines 1-4).

Dehaine et al. teach a BGA package comprising a frame and a heat dissipating support plate (13 and 17 respectively in Fig. 1 and 3A/3C) where the frame is divided/split into four rings/sections of conductive planes (Q1-Q4 in Fig. 3A/3C) such that each ring/section is separated from each other by an insulating strip (23 in Fig. 3A/3C; Col. 10, line 57) and each ring/section can be electrically connected to different signal potentials/functions such as ground, desired voltage, etc. (see a ground ring 24 in Fig. 3A; Col. 11, line 9) in order to achieve the desired signal transmission and power decoupling functions (Col. 10, line 52- Col. 11, line 18).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the stiffener including a copper (Cu) ring split into power and ground portions having an insulating couplers arranged to mechanically secure, while electrically isolating the power and ground portions of the Cu as taught by the embodiments of Fig. 13 and 14 in Dibene, II et al. ('113 patent) and Dehaine et al. so that the desired ground/voltage routing and mechanical coupling can be achieved and the signal noise/interference can be reduced in Dibene, II et al's ('113 and '804 patents) package.

Regarding claim 3, Dibene, II et al. ('113 and '804 patents) teach substantially the entire claimed structure as applied to claims 1 and 2 above, wherein Dibene, II et al. further teach the conductive surfaces/paths being bonded/mounted on the substrate via conventional solder bonding to provide a low resistance/high current path and to remove heat from the substrate (Col. 10, lines 20-26; Col. 11, lines 9-15).

7. Claim 8 insofar as being in compliance 35 U.S.C. 112, is rejected under 35 U.S.C. 103(a) as being unpatentable over Dibene, II et al. ('113 and 804 patents) as applied to claims 1 and 2 above, and further in view of Dehaine et al. (US Pat. 5925925) and Banks et al. (US Pat. 6015722).

Regarding claim 8, Dibene II et al. ('113 and 804 patents) and Dehaine et al. teach substantially the entire claimed structure as applied to the claims 1 and 2 above, except using a thermal interface material and an epoxy to bond the heat spreader plate to the split copper ring and the die respectively.

Dibene II et al. ('113 patents) further teach a heat sink/heat spreader plate assembly (1006/1010/1004 in Fig. 10-11B) being bonded to the PCB/package frame and the IC die using a thermal interface material such as a thermal grease (Col. 9, line 40-67).

Banks et al. teach a heat dissipative flip chip package where a lid/heat spreader plate is bonded to a copper ring/stiffener (532 and 522 in Fig. 9) using a conventional adhesive material such as an epoxy (538 in Fig. 9; Col. 28, line 2) to provide the desired adhesion and moisture protection (Col. 26, line 30- Col. 28, line 28).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the thermal interface material and the epoxy to bond the heat spreader plate to the split copper ring and the die respectively as taught by Banks et al. so that the adhesion and moisture protection can be improved in Dehaine et al. and Dibene, II et al's ('113 and 804 patents) package.

Response to Arguments

8. Applicant's arguments with respect to claims 1-9 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Reference C is cited as being related to a package having a split conductive ring structure.

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 703-305-3410. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 703-308-1690. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-306-3431.

Nitin Parekh
NP
10-10-03

A handwritten signature in black ink, appearing to read 'Eddie Lee', with a large, sweeping initial 'E'.

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800